

IN THE SPECIFICATION

Please amend the specification as follows:

Page 2, line 1, amend the paragraph in the section "CROSS REFERENCE TO RELATED APPLICATION" previously added by preliminary amendment as follows:

"This application claims the benefit and is a continuation of U.S. Patent Application No. 09/475,105, filed December 30, 1999 by Jonathan Douglas et al., now ~~allowed~~ issued as U.S. Pat. No. 6,609,193."

Page 26, line 12, amend the paragraph beginning there-at and continuing over to page 27, line 5 (corresponding to Para. [0047] of the published application) as follows:

"A bubble is a number of invalid instructions located within the instruction decoder. Usually the bubble is created as a result of an entire thread of instructions mixed amongst other instruction threads in the instruction decode pipeline becoming invalid. An example that would cause this is a misconnected branch. The bubble squeeze algorithm performed by the present invention generally squeezes out the bubbles of invalid instructions in the instruction decode pipeline. The bubble squeeze algorithm is essentially accomplished by continuing to clock pipestages which have their instructions marked as invalid until a valid instruction is received. The clocks to a pipestage containing a valid instruction are temporarily stopped until the

reason for the stall is cleared. The invalid instructions are eventually squeezed out by writing valid instructions over the invalid instructions stored in the pipestages. The bubble squeeze algorithm continues to run the instruction decode pipeline to bring instructions of other threads further down the pipeline instead of performing a non-intelligent or blocking stall. Bubble squeezing can provide greater throughput in the instruction decoder."

Page 63, amend the paragraph in the section ABSTRACT OF THE DISCLOSURE as follows:

"A ~~multithread~~ pipelined instruction decoder for a multithread processor including an instruction decode pipeline, a valid bit pipeline, and a thread identification pipeline in parallel together, with each having the same predetermined number of pipe stages. ~~to clock, clear and stall an~~ The instruction decode pipeline of a multi-threaded machine to decode instructions associated with a plurality of instruction threads. ~~maximize performance and minimize power. A shadow~~ The valid bit pipeline to associate a valid indicator at each pipe stage with each instruction being decoded in ~~shadows~~ the instruction decode pipeline. The thread identification pipeline to associate ~~maintaining a the thread-identification and instruction-valid bits~~

~~for at each pipestage with each instruction being decoded in of~~
~~the instruction decoder decode pipeline.~~ The ~~thread-id and valid~~
~~bits are used to control the clear, clock, and stall of each~~
~~pipestage of the pipelined instruction decoder may further include~~
~~a pipeline controller to control the clocking of each pipe stage~~
~~of .~~ Instructions of one thread can be cleared without
~~impacting instructions of another thread in the instruction decode~~
~~pipeline, the valid bit pipeline, and the thread identification~~
~~pipeline.~~ In some cases, instructions of one thread can be
~~stalled without impacting instructions of another thread in the~~
~~decode pipeline.~~ In the present invention, pipestages are clocked
~~only when a valid instruction needs to advance in order to~~
~~conserve power and to minimize stalling."~~ The pipeline controller
~~may invalidate an entire thread of instructions, squeeze out~~
~~invalid instructions, and/or conserve power by selectively~~
~~stopping the clocking of pipestages.~~